Low K dielectric integrated circuit interconnect structure

FIELD OF THE INVENTION

The invention is generally related to the field of semiconductor processing and more specifically to method for forming a low K dielectric structure.

BACKGROUND OF THE INVENTION

As the operating speeds of integrated circuits increase, it is becoming increasingly important that any capacitance associated with the metal interconnect lines that form the integrated circuit be reduced. Currently, the metal interconnect lines that connect the various electronic components are embedded in dielectric layers formed above a semiconductor. Parasitic capacitance is introduced into the integrated circuit by the metal interconnect lines and the inter-metallic dielectric (IMD) layers. The capacitance of these structures is proportional to the dielectric constant of the IMD layers that comprise the interconnect structure. One method of reducing the

parasitic capacitance is to use dielectric material with a low dielectric constant (i.e. low K dielectric material) to form the IMD layers. An example of such a structure is shown in Figure 1.

As shown in Figure 1, a low K dielectric layer 20 is formed above a semiconductor 10. Although omitted from the Figure, any number of intervening layers can be formed between the semiconductor 10 and the dielectric layer 20. In some cases a barrier layer 30 is formed on the low K dielectric layer 20. Most high performance integrated circuits use copper to form the metal interconnects. Copper lines are typically formed using a damascene-type process in which a trench is first formed in the dielectric. The trenches are then filled with copper using a copper electroplating process. As shown in Figure 1, trenches 36, 36 are formed in the dielectric layer 20. A lined layer 40 is formed in the trench prior to the formation of the copper lines. The liner typically comprises tantalum nitride or other similar material. The low K dielectric material used to form the dielectric layer 20 is a porous material and typically comprises an open pore structure. During the formation of the liner layer 40, the material used to form the liner layer 40 will penetrate into the low

K dielectric material resulting in the formation of regions of liner material 50 in the low K dielectric material 20. Following the formation of the liner layer 40, the trenches 34, 36 are filled with copper 45 to form the interconnect lines. In the case of adjacent trenches it is possible that the liner material can form a path 60 that connects the trenches. If the liner material is electrically conductive then an electrical short will exist between the copper lines in the adjacent trenches. This electrical short can cause the integrated circuit to malfunction or cease to operate.

There is therefore a need for a method to form interconnect structures using low K dielectric material that will not result in the formation of electrical shorts. The instant invention addresses this need.

SUMMARY OF THE INVENTION

The instant invention comprises a structure and method for forming integrated circuit copper interconnects. A low K dielectric layer is formed over a semiconductor. Trenches are formed in the dielectric layer and a first contiguous barrier layer is formed in the trenches using ALD, CVD, or PVD. The thickness of the barrier layer over the upper surface of the low K dielectric layer is X1 and the thickness of the barrier layer formed along the sidewalls of the trenches is X_2 where $X_1 > X_2$. An optional second barrier layer can be formed over the first contiguous barrier layer. Copper is then used to fill the trenches and form the interconnect structure.

The instant invention offers the advantage of reducing the penetration of the barrier layer material into the low K dielectric. This and other advantages will be apparent to those of ordinary skill in the art having reference to the specification in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIGURE 1 is a cross sectional diagram showing the creation of electrical shorts in the interconnect structure of an integrated circuit according to the prior art.

FIGURES 2(a)-2(b) are cross sectional diagrams showing an embodiment of the instant invention.

FIGURE 3 is a cross sectional diagram showing a further embodiment of the instant invention.

Common reference numerals are used throughout the Figures to represent like or similar features. The Figures are not drawn to scale and are merely provided for illustrative purposes.

DETAILED DESCRIPTION OF THE INVENTION

While the following description of the instant invention revolves around Figure 2(a), Figure 2(b), and Figure 3, the instant invention can be utilized in any integrated circuit. The methodology of the instant invention provides an improved interconnect structure and method for integrated circuit formation.

As shown in Figure 2(a), a low K dielectric layer 20 is formed above a semiconductor 10. Any number of intervening layers can be formed between the semiconductor 10 and the low K dielectric layer 20. Some of these intervening layers will include metal lines and addition dielectric layers. Electronic devices such as transistors, diodes, etc. will be formed in the semiconductor 10 and have been omitted from all the Figures for clarity. Low K dielectric material used to form layer 20 is defined for purposes of this invention as dielectric material with a dielectric constant of approximately $\leq$ 3.7. The term low K dielectric is also intended to include dielectric material with a dielectric constant of $\leq$ 3.2. The term low K dielectric is also intended to include the class of ultra-low K dielectric material which is defined as dielectric

material with a dielectric constant of $\leq$ 2.5. Various embodiments of the instant invention can include the following low K and ultra-low K dielectric materials: silsesquioxane (SSQ)-based materials, e.g., methylsilsesquioxane (MSQ), or hydrogensilsesquioxane (HSQ), silica-based materials, e.g., carbon- or fluorine-doped silica glasses, organic-polymer-based materials, amorphous-carbon-based materials, and any other dielectric material that can be made with porous characteristics to reduce the dielectric constant. In general low K dielectric material has pores that can be described as open spaces within the dielectric material. In an embodiment the pores in the low K dielectric layer can comprise an average pore size (or pore diameter) of 1nm or larger. In a further embodiment the pores in the low K dielectric layer can comprise an average pore size (or pore diameter) of 2nm or larger.

Formed on the low K dielectric layer 20 is a barrier layer 30. In an embodiment of the instant invention the barrier layer 30 comprises silicon nitride or other suitable dielectric material. Following the formation of the low K dielectric layer 20 and any barrier layer 30, a patterned photoresist is formed on the structure and used

as an etch mask during the etching of the dielectric layer 20 and the barrier layer 30 to form the trenches 80, 85.

Following the formation of the trenches 80, 85, a contiguous liner layer (or barrier layer) is formed in the trenches 80, 85. The liner layer or barrier layer can be formed using atomic layer deposition, physical vapor deposition, or chemical vapor deposition methodologies. Shown in Figure 2(a) is a contiguous liner or barrier layer 70 formed according to an embodiment of the instant invention. In this embodiment a non-conformal barrier layer 70 is formed in which the thickness X_1 is greater than X_2. In an embodiment X_1 represents the thickness of the non-conformal layer 70 formed over the upper surface 35 of the low K dielectric layer 20 and X_2 represents the thickness of the non-conformal barrier layer 70 on a sidewall 83 of the trenches. The liner or barrier layer 70 can comprise titanium, tungsten, tantalum, titanium nitride, tantalum nitride, tungsten nitride, titanium silicon nitride, tantalum silicon nitride, tungsten silicon nitride, ruthenium, iridium, and any alloys that comprise these materials. A number of deposition methods such as chemical vapor deposition (CVD), atomic layer deposition (ALD), and

physical vapor deposition (PVD) can be used to form the layer 70.

In the case of CVD (and similar for ALD) processes, the non-conformal layer 70 of the instant invention can be formed by moving from a surface-reaction limited deposition regime to a more mass transport limited deposition regime where, for example, higher substrate temperatures or lower precursor flow rates/partial pressures of the chemical reactants can starve the reactants resulting in the non-conformal layers 70 shown in Figure 2(a). The reduction (or starving) of reactants used to deposit the barrier layer 70 will result in the limited penetration of the barrier layer material into the pores that exist along the vertical low K dielectric surfaces 83 of the trenches 80, 85. The reduced penetration of the barrier material is indicated 55 in Figure 2(a) and Figure 2(b). For PVD processes an increase in the ionic-flux distribution (or wider flux distribution) will result in non-conformal barrier layer 70 formation. In addition, the PVD process can be adjusted to increase the re-sputter component of the deposited barrier liner material onto the sidewalls 83 to paste further barrier material onto the sidewalls for an additional pore-sealing effect.

As shown in Figure 2(a), adjacent trenches 80, 85 can be formed in the integrated circuit. In an embodiment of the instant invention, the width X_4 of the dielectric separating adjacent trenches is less than or equal to 160nm. In a further embodiment the width X_3 of the adjacent trenches is each less than or equal to 160nm. In Figure 2(a) only two adjacent trenches are shown. The instant invention is not to be limited to two adjacent trenches. The instant invention covers any number of adjacent trenches or via structures formed in low K dielectric material.

In an embodiment of the instant invention, the ratio of X_1 to X_2 (i.e. X_1/X_2) for the case where CVD or ALD is used to form the barrier layer 70 is greater than 3 to 2 (i.e. 3/2). In a further embodiment, the ratio X_1/X_2 for the case where CVD or ALD is used to form the layer 70 is greater than 5/2. In a further embodiment, CVD or ALD can be used to form the barrier layer 70 in the above described ratios when X_3 is less than or equal to 160nm and/or X_4 is less than or equal to 160nm.

In a further embodiment of the instant invention, the ratio of X_1 to X_2 (i.e. X_1/X_2) for the case where PVD is used to form the barrier layer 70 is greater than 3 to 1 (i.e. 3/1). In a further embodiment, the ratio X_1/X_2 for the case where PVD is used to form the layer 70 is greater than 8/1. In a further embodiment, PVD can be used to form the barrier layer 70 in the above described ratios when X_3 is less than or equal to 160nm and/or X_4 is less than or equal to 160nm.

As shown in Figure 2(b), copper 100 is used to fill the trenches 80, 85 following the formation of the barrier or liner layer 70. The copper structures can be formed using any known method of copper line formation. In an embodiment of the instant invention, copper is formed in the trenches 80, 85 using an electroplating technique. Any excess copper is removed from the surface of the structure using chemical mechanical polishing (CMP).

Shown in Figure 3 is a further embodiment of the instant invention. As shown in the Figure, a low K dielectric layer 20 is formed over a semiconductor 10. Adjacent trenches 110, 120 are formed in the low K dielectric layer 20 as described above. The embodiment

shown in the Figure should not be limited to two adjacent trenches. The embodiment is intended to apply to a single trench or to any number of adjacent trenches that are formed in the low K dielectric layer 20. A first non-conformal barrier layer 70 is formed in the trenches 110 and 120 using PVD, ALD or CVD. If PVD is used to form the layer 70, the thickness ratio X_1/X_2 is greater than 3/1 in a first embodiment and greater than 8/1 in a second embodiment. If CVD or ALD is used to form the layer 70, the thickness ratio X_1/X_2 is greater than 3/2 in a first embodiment and greater than 5/2 in a second embodiment. The liner or barrier layer 70 can comprise titanium, tungsten, tantalum, titanium nitride, tungsten nitride, tantalum nitride, titanium silicon nitride, tungsten silicon nitride, tantalum silicon nitride, ruthenium, iridium, and any alloys that comprise these materials. Following the formation of the barrier or liner layer 70, a second barrier or liner layer 130 is formed over the layer 70. The second barrier or liner layer 130 can comprise titanium, tungsten, tantalum, titanium nitride, tungsten nitride, tantalum nitride, titanium silicon nitride, tungsten silicon nitride, tantalum silicon nitride, ruthenium, iridium, and any alloys that comprise these materials. In an embodiment, the second barrier or liner layer 130 can be

a conformal layer where the layer thickness X_6 is approximately equal to the layer thickness X_7. In a further embodiment the second layer 130 can be a non-conformal layer where the layer thickness X_6 is greater than the layer thickness X_7. In either embodiment the second layer 130 can be formed using ALD, CVD, PVD, or any other suitable technique. If PVD is used to form the second layer 130, the thickness ratio X_6/X_7 is greater than 3/1 in a first embodiment and greater than 8/1 in a second embodiment. If CVD or ALD is used to form the layer 130, the thickness ratio X_6/X_7 is greater than 3/2 in a first embodiment and greater than 5/2 in a second embodiment. In a further embodiment of the instant invention, additional barrier or liner layers can be formed on the second layer 130. The additional layers can be conforming or non-conforming and can comprise titanium, tungsten, tantalum, titanium nitride, tungsten nitride, tantalum nitride, titanium silicon nitride, tungsten silicon nitride, tantalum silicon nitride, ruthenium, iridium, and any alloys that comprise these materials. Following the formation of the second layer 130, and any additional layers, copper 100 is used to fill the trenches 110, 120.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention will be apparent to persons skilled in the art upon reference to the description. For example, in cases where a barrier trench overhang forms on the top surface of the dielectric adjacent to the trench, the overhang can be removed using an insitu barrier etch (e.g., etch in dep/etch/dep (DED) sequence) to "clip-off" the over-deposition. It is therefore intended that the appended claims encompass any such modifications or embodiments.